a conductive region within said trench adjacent said insulating layer;

a body region of a second conductivity type provided within an upper portion of said epitaxial layer and adjacent said trench;

a source region of said first conductivity type provided within an upper portion of said body region and adjacent said trench;

an upper region of second conductivity type within an upper portion of said body region and laterally adjacent said source region, wherein said upper region does not extend to said trench, and wherein said upper region has a higher majority carrier concentration than said body region; and

a source contact region disposed on said epitaxial layer upper surface, said source contact region comprising: (a) a doped polycrystalline silicon contact region in electrical contact with said source region and (b) a metal contact region adjacent said doped polycrystalline silicon contact region and in electrical contact with said source region and with said upper region.

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16. (Amended) A trench MOSFET transistor device comprising:

an N-type silicon substrate;

an N-type silicon epitaxial layer over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate;

a trench extending into said epitaxial layer from an upper surface of said epitaxial layer;

a silicon oxide insulating layer lining at least a portion of said trench;

a doped polycrystalline silicon conductive region within said trench adjacent said insulating layer;

a P-type body region provided within an upper portion of said epitaxial layer and adjacent said trench;

an N-type source region provided within an upper portion of said body region and adjacent said trench;

a P-type upper region within an upper portion of said body region and laterally adjacent said source region, wherein said upper region does not extend to said trench, and wherein said upper region has a higher majority carrier concentration than said body region;

a borophosphosilicate glass insulating region disposed over said conductive region, said insulating region extending above said epitaxial layer upper surface; and

a source contact region disposed on said epitaxial layer upper surface and laterally adjacent said insulating region, said source contact region comprising: (a) a doped polycrystalline silicon contact region having N-type doping and (b) a metal contact region adjacent said doped polycrystalline silicon contact region and in electrical contact with said source region and with said upper region.

REMARKS

Claims 1-16 are pending in the application with Claims 17-21 withdrawn from consideration due to a restriction requirement. Claims 1 and 16, the only independent claims, have been amended herein. Attached hereto, captioned "**Version with markings to show changes made**", is a marked-up version of the changes made to the claims.

Claims 1-16 were rejected under Section 103(a) as being unpatentable over US Patent 4,893,160 (Hshieh et al.) in view of US Patent 6,251,730 (Luo) and Claim 10 was rejected as being unpatentable over Hshieh in view of Luo and further in view of Applicants' alleged admitted prior art (APA) in figs. 1 and 2. Each of the rejections is respectfully traversed and reconsideration is requested.

Each of independent Claims 1 and 16 has been amended to further distinguish over the cited art. Specifically, each now recites that the trench MOSFET transistor device has an upper region of second conductivity type within an upper portion of the body region and *laterally* adjacent the source region, *wherein the upper region does not extend to the trench*, and wherein the upper region has a higher majority carrier concentration than the body region.